IN THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) A frequency monitor circuit (FMC) ~~that is configured to be part of an integrated circuit chip and~~ configured to receive at least one monitored clock whose frequency is to be monitored, ~~each of said clocks being a respective monitored clock,~~ said FMC comprising:

a reference window generator (RWG), operative to output a reference window signal defining a reference window, the reference window having a given duration;

a monitored clock counter (MCC), responsive to said reference window signal and to any one of the at least one monitored clock [[s]] and operative to count all pulses in the respective monitored clock that occur within the duration of said reference window and to output a corresponding pulse count; and

at least two comparators, responsive to said pulse count, each comparator being operative to compare said pulse count with a respective given threshold value and to output a corresponding indication of frequency deviation.

2. (Currently Amended) The frequency monitor circuit of claim 1, further comprising a storage and logic module (SLM), responsive to outputs of said comparators, wherein said [[RCC]] RWG, said MCC and said comparators are operative to function repeatedly and the SLM is operative to store one or more indications output by the comparators, the stored indications being available for readout.

3. (Currently Amended) The frequency monitor circuit of claim 2, wherein said SLM is further operative to process the stored indications so as to obtain statistical information about the frequency of any of the at least one monitored clock [[s]].

4. (Original) The frequency monitor circuit of claim 3, wherein said statistical information includes indication of a trend in frequency deviation.

5. (Currently Amended) The frequency monitor circuit of claim 1, formed on an integrated circuit chip that includes at least one clock generator, [[the]] an output of any of said at least one clock generator [[s]] being one of the at least one monitored clock [[s]].

6. (Currently Amended) The frequency monitor circuit of claim 5, wherein said [[any]] at least one clock generator comprises a phased locked loop (PLL).

7. (Currently Amended) The frequency monitor circuit of claim 5, wherein said [[any]] at least one clock generator is a frequency multiplier.

8. (Original) The frequency monitor circuit of claim 7, wherein said RWG and said MCC form part of said frequency multiplier.

9. (Currently Amended) The frequency monitor circuit of claim 1, further configured to be receptive to a reference clock and wherein said RWG includes a reference clock counter (RCC), responsive to the reference clock and operative to count a given number of reference clock pulses and wherein [[the]] a beginning of said reference window coincides with [[the]] a beginning of said counting and [[the]] an end of said reference window coincides with [[the]] an end of said counting.

10. (Currently Amended) The frequency monitor circuit of claim 9, wherein [[the]] an integrated circuit chip includes a clock generator of [[the]] a frequency multiplier type, whose output is a monitored clock, wherein said RCC and said MCC form part of said clock generator.

11. (Original) The frequency monitor circuit of claim 1, wherein said at least one clock is at least two clocks, the FMC further comprising a selector, receptive to the monitored clocks and operative to switch any one of them into said MCC.

12. (Original) The frequency monitor circuit of claim 11, formed on an integrated circuit chip that forms part of a digital system and at least one of the monitored clocks is input to the chip.

13. (Original) The frequency monitor circuit of claim 11, wherein the duration of said reference window is different for each monitored clock.

14. (Original) The frequency monitor circuit of claim 11, wherein, for any of said comparators, the respective threshold value is different for each monitored clock.

15. (Currently Amended) An integrated circuit chip, on which there is provided at least one monitored clock whose frequency is to be monitored, ~~each of said clocks being a respective monitored clock,~~ the chip comprising a frequency monitor circuit (FMC) that includes:

a reference window generator (RWG), operative to output a reference window signal defining a reference window, the reference window having a given duration;

a monitored clock counter (MCC), responsive to said reference window signal and to any one of the at least one monitored clock [[s]] and operative to count all pulses in the respective monitored clock that occur within the duration of said reference window and to output a corresponding pulse count; and

at least two comparators, responsive to said pulse count, each comparator being operative to compare said pulse count with a respective given threshold value and to output a corresponding indication of frequency deviation.

16. (Currently Amended) The integrated circuit chip of claim 15, wherein said FMC further includes a storage and logic module (SLM), responsive to outputs of said comparators, wherein [[RCC]] said RWG, said MCC and said comparators are operative to function periodically and the SLM is operative to store [[any]] one or more indications output by the comparators, the stored indications being available for readout.

17. (Currently Amended) The integrated circuit chip of claim 16, wherein said SLM is further operative to process the stored indications to obtain statistical information about the frequency of any of the at least one monitored clock [[s]].

18. (Original) The integrated circuit chip of claim 17, wherein said statistical information includes indication of a trend in frequency deviation.

19. (Currently Amended) The integrated circuit chip of claim 15, further including at least one clock generator and wherein [[the]] an output of any of said at least one clock generator [[s]] is one of the at least one monitored clock [[s]].

20. (Currently Amended) The integrated circuit chip of claim 19, wherein said at least one clock generator includes a phase locked loop (PLL).

21. (Currently Amended) The integrated circuit chip of claim 19, wherein said at least one clock generator is a frequency multiplier.

22. (Original) The integrated circuit chip of claim 21, wherein said RWG and said MCC form part of said frequency multiplier.

23. (Currently Amended) The integrated circuit chip of claim 15, wherein there is further provided on the chip a reference clock and wherein said RWG includes a reference clock counter (RCC), responsive to the reference clock and operative to count a given number of reference clock pulses and wherein [[the]] a beginning of said reference window coincides with [[the]] a beginning of said counting and [[the]] an end of said reference window coincides with [[the]] an end of said counting.

24. (Currently Amended) The integrated circuit chip of claim 23, further including a clock generator of [[the]] a frequency multiplier type, whose output is a monitored clock, wherein said RCC and said MCC form part of said clock generator.

25. (Original) The integrated circuit chip of claim 15, wherein said at least one clock is at least two clocks, the FMC further comprising a selector, responsive to the monitored clocks and operative to switch any one of them into the MCC.

26. (Original) The integrated circuit chip of claim 25, the chip forming part of a digital system and at least one of the monitored clocks being generated, within the system, outside the chip.

27. (Original) The frequency monitor circuit of claim 25, wherein the duration of said reference window is different for each monitored clock.

28. (Original) The frequency monitor circuit of claim 25, wherein, for any of said comparators, the respective threshold value is different for each monitored clock.